

Amendment to Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended)

A non-volatile memory cell structure, said non-volatile memory cell structure comprising:

an N-type well region in a substrate, a channel region between a P-type source region and a P-type drain region, wherein the conductivity type of said P-type is opposite to the conductivity type of said N-type;

a first insulator layer on the surface of said N-type well region;

a floating gate overlying said first insulator layer;

a second insulator layer on said floating gate; and

a control gate on said second insulator layer, wherein said non-volatile memory cell is erased by applying an erase voltage to said P-type drain region, a supply voltage to said control gate, and said erase voltage to said N-type well region[.].

Claim 2 (Cancelled)

Claim 3 (Previously Presented)

The non-volatile memory cell structure according to claim 1, further comprising a source line coupled to said P-type source region, said source line exhibits floating.

Claim 4 (Previously Presented)

The non-volatile memory cell structure according to claim 3, wherein said source line is divided by an isolation structure along a bit line direction.

Claim 5 (Previously Presented)

A semiconductor memory cell structure, said semiconductor memory cell structure comprising:

an N-type well region in a substrate, a channel region between a P-type drain region and a P-type source region, wherein the conductivity type of said N-type is opposite to the conductivity type of said P-type;

an insulator layer overlying said N-type well region; and

a gate transistor on said insulator layer, said gate transistor comprises a control gate coupled to a word line, said P-type drain region coupled to a bit line, wherein said cell is erased by applying an erase voltage to said N-type well region, and applying a supply voltage to said control gate.

Claim 6 (Previously Presented)

The semiconductor memory cell structure according to claim 5, wherein said P-type source region is coupled to a source line.

Claim 7 (Previously Presented)

The semiconductor memory cell structure according to claim 6, wherein said source line is divided by an isolation structure along a bit line direction.

Claim 8 (Previously Presented)

The semiconductor memory cell structure according to claim 5, wherein said supply voltage applied to said control gate is erase voltage.

Claim 9 (Currently Amended)

The semiconductor memory cell structure according to claim 5, wherein said cell is programmed by applying a negative supply voltage around $[-6 \text{ to } -10]$ -4 to -6 volts to said P-type drain region to induce hot electrons, and a negative threshold voltage is of about -4 volts applied to said word line.

Claim 10 (Previously Presented)

A method for erasing non-volatile memory cell having a P-type substrate and an N-type well region therein, a channel region between a P-type drain region and a P-type source region, said method comprising the steps of:

applying an erase voltage to said P-type drain region to cause tunneling oxide layer of electrons floats from a floating gate to said N-type well region, wherein said P-type drain region coupled to a bit line;

applying a supply voltage to a control gate, wherein said control gate coupled to a word line; and

grounding said word line of unselected cell and said bit line of unselected cell to cause said P-type drain region as an inhibit switch.

Claim 11 (Cancelled)